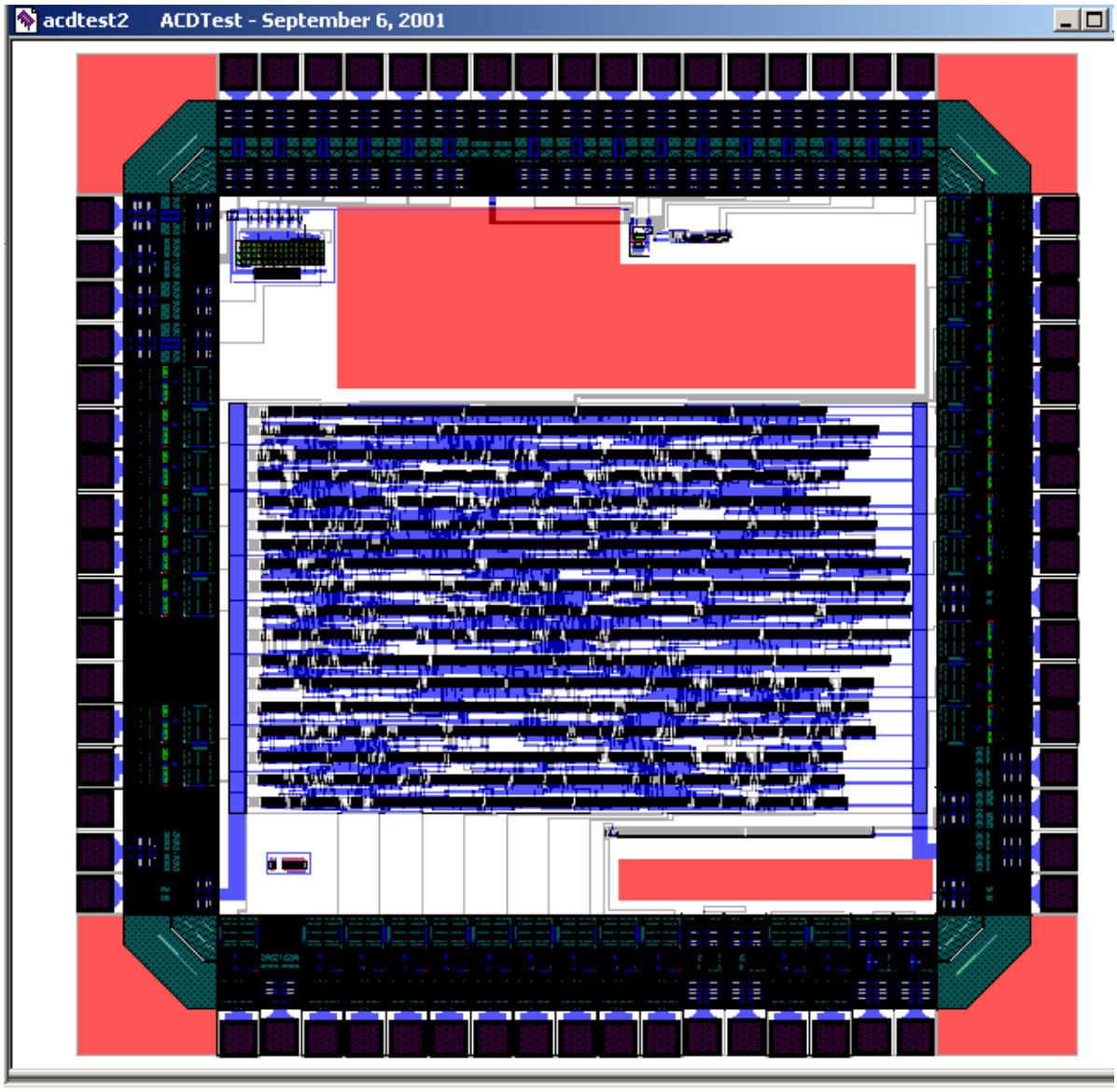
ACDTEST2 ASIC Test Report
November 2001



This Test Report is for ASIC “ACDTEST2” submitted to MOSIS on 9-10-01 as job 63156 and received back at GSFC on 11-06-01. Testing from 11-06-01 through 11-13-01. The original schedule date for part receipt was listed as 12-14-01.

This device was fabricated by MOSIS in the Agilent HP_AMOS14TB 0.5 μm process on run T19M. This project cost $5185 for the minimum size and minimum quantity of devices.

We received 5 die packaged in a pin grid array PGA84M package and 20 unpackaged die. A photo of the packaged part is shown below. The die size is 2.13 mm^2. There are 68 bond pads on 90 μm centers. As seen below in Fig. 1, automated bonding was successfully accomplished with 1 mil aluminum wedge bonds.

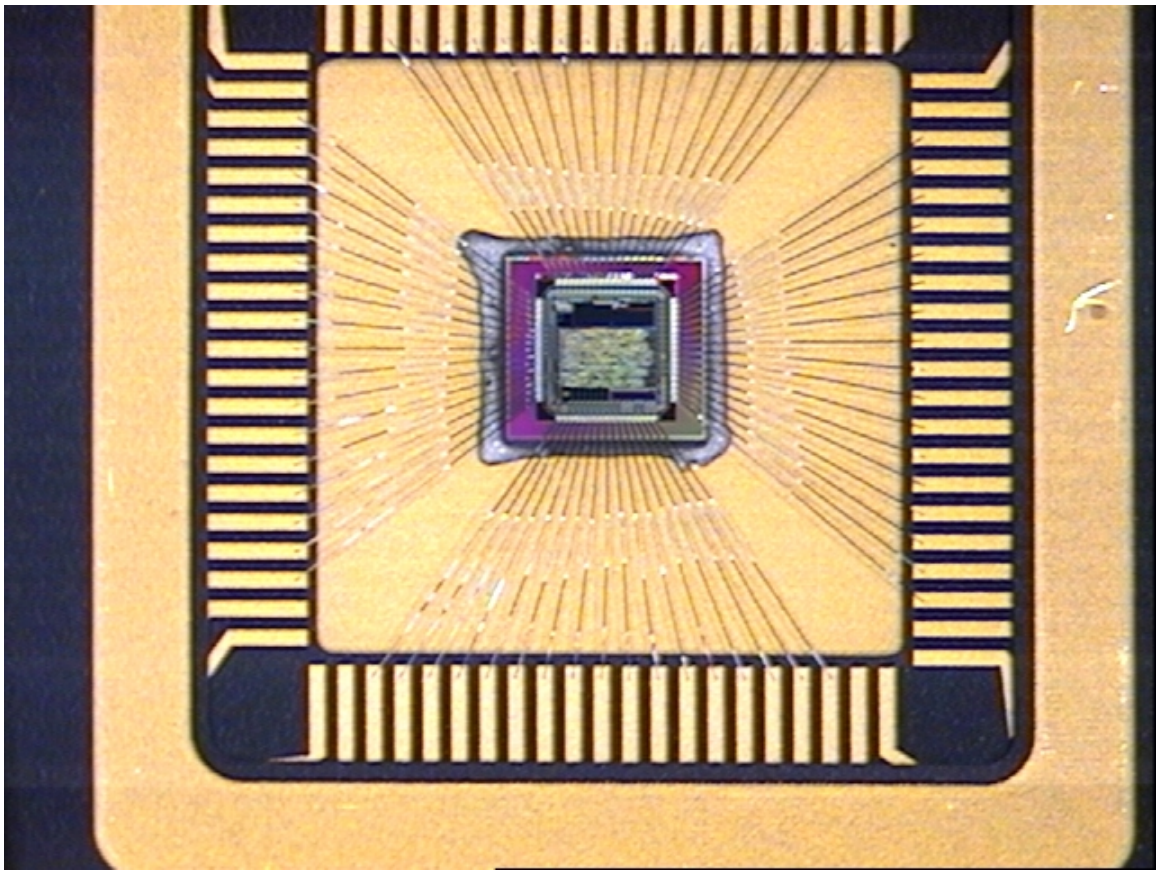


Fig. 1

There were several goals to be accomplished with the fabrication of this ASIC. These include:

1. Verification of the Exemplar Leonardo Spectrum (v2001_1b.12) synthesis toolset using the Agilent 0.5 μm library
2. Verification of the Tanner V8.30 layout toolset and standard cell library, including the automated place and route function.
3. Verification of our process of transferring GDSII data from LHEA to MOSIS.
4. Verification of the "mtest" logic module designed by Bob Baker

5. Verification of the ESD protection pads and IO buffers provided by the Tanner toolset. Verification of the pad frame setup designed at GSFC.
6. Test of a GSFC-designed 101 stage ring oscillator.
7. Test of the SLAC-provided digital-to-analog converter
8. Test of the SLAC-provided LVDS driver and receiver circuitry
9. Test of chip-to-chip variations in a GSFC-designed poly resistor

A closer view of the ACDTEST2 chip is shown below in Fig. 2 (the first version of the design, ACDTEST1, was never fabricated). The DAC is in the upper left corner. The LVDS circuitry is at the top-middle of the IC. The "mtest" logic is the large block in the center of the chip. The ring oscillator, poly resistor, and IO buffer test circuitry is at the lower right. The large block of poly at the top and on the outer ring are grounded. These are in place to meet the minimum poly density requirements of the Agilent process.

These ASICs were tested at the LHEA by Bob Baker and Dave Sheppard in Nov. 2001. ASIC #1 was used for the majority of the testing.

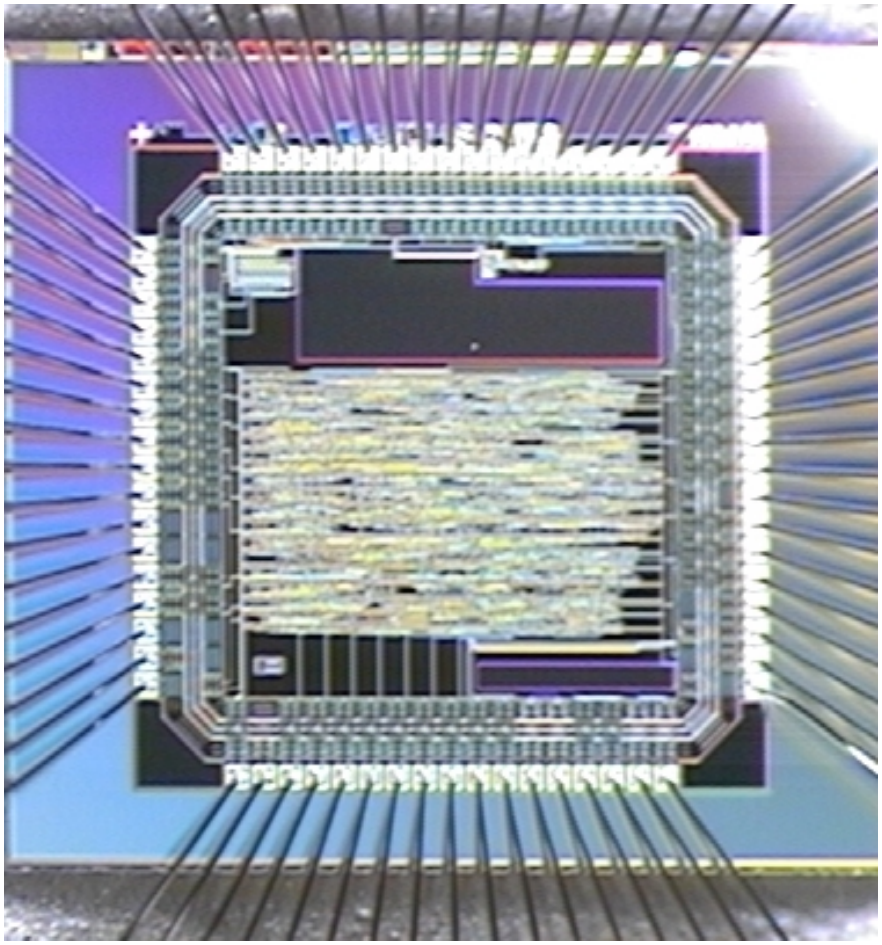


Fig. 2

Test of the MTEST Logic:

The “mtest” logic module is a set of 8 pseudo-random pattern generators and sync modules. The PR pattern generator starts with a seed bit of 1 in register bit 0 (via reset) in a 16 bit shift register and uses the following feedback mechanism for each of the 8 identical circuits.

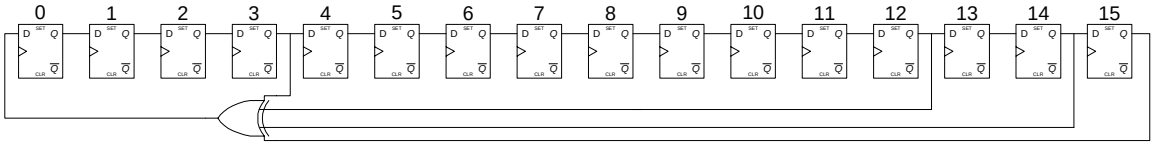


Fig. 3

The block produces a sync pulse either when the 16 bit pattern = 16’hEB90. This pattern in operation is shown on the scope plot below. The sync pulse is shown on channel 2 and the data stream (Q15) is shown on channel 1 below in Fig. 4.

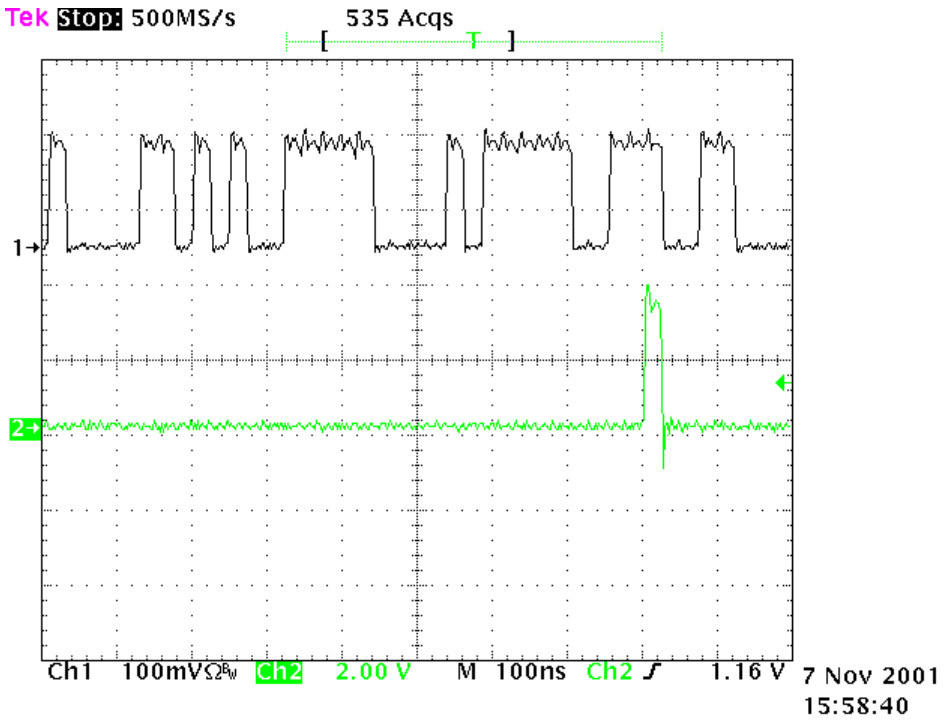
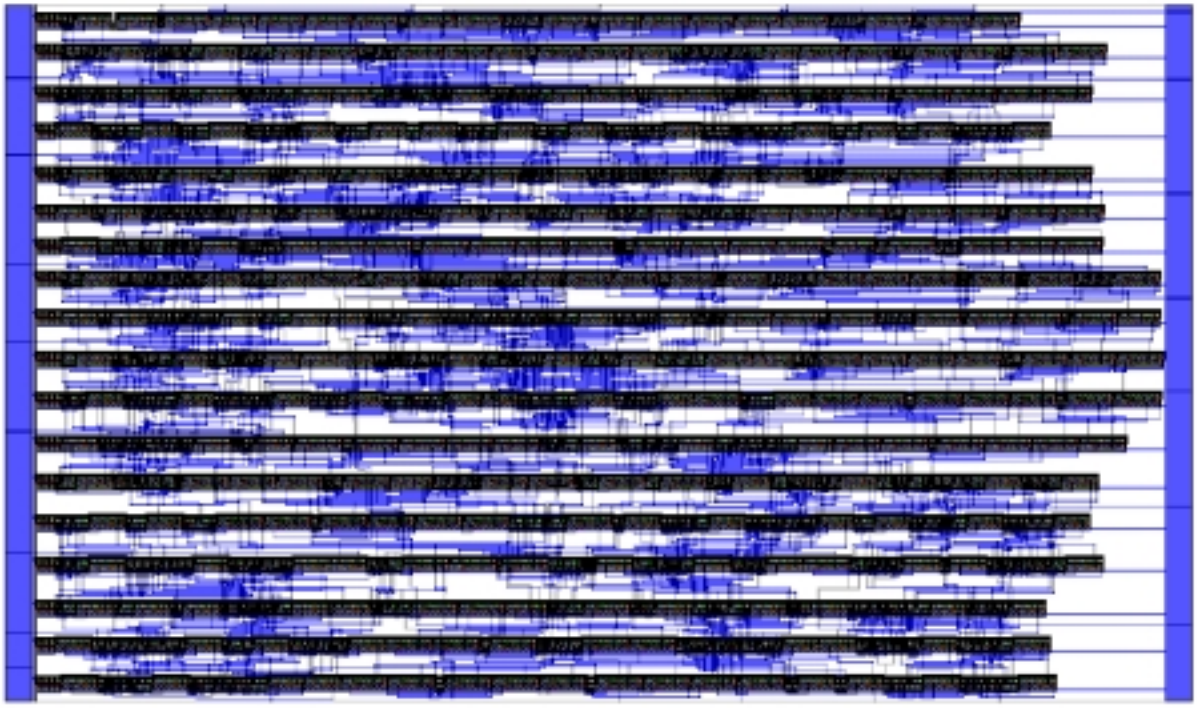


Fig. 4

The following “mtest” logic block was produced from using the automated place and route tools in Tanner.



MTEST Logic, Fig. 5

The MTEST logic module was found to work as designed in preliminary testing. All eight sync pulses were operational.

Digital to Analog Converter

The digital-to-analog converter module (plus some added circuitry) delivered from SLAC is shown below in Fig. 6. The switch positions used for our test are labeled, from left to right on the inverters shown below, D1 – D6 (e.g., pins K1 – J1 – H2 – H1 – G3 – G2), where D6 is the MSB.

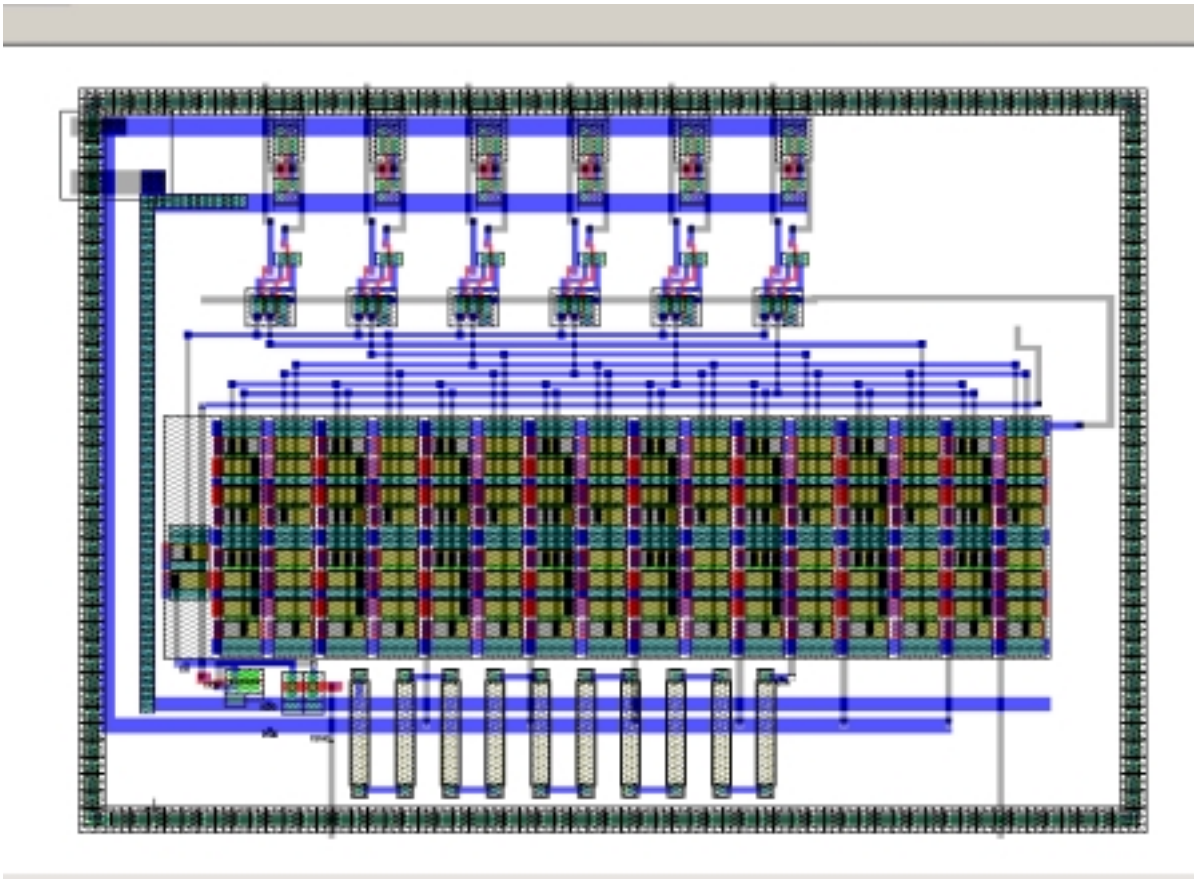
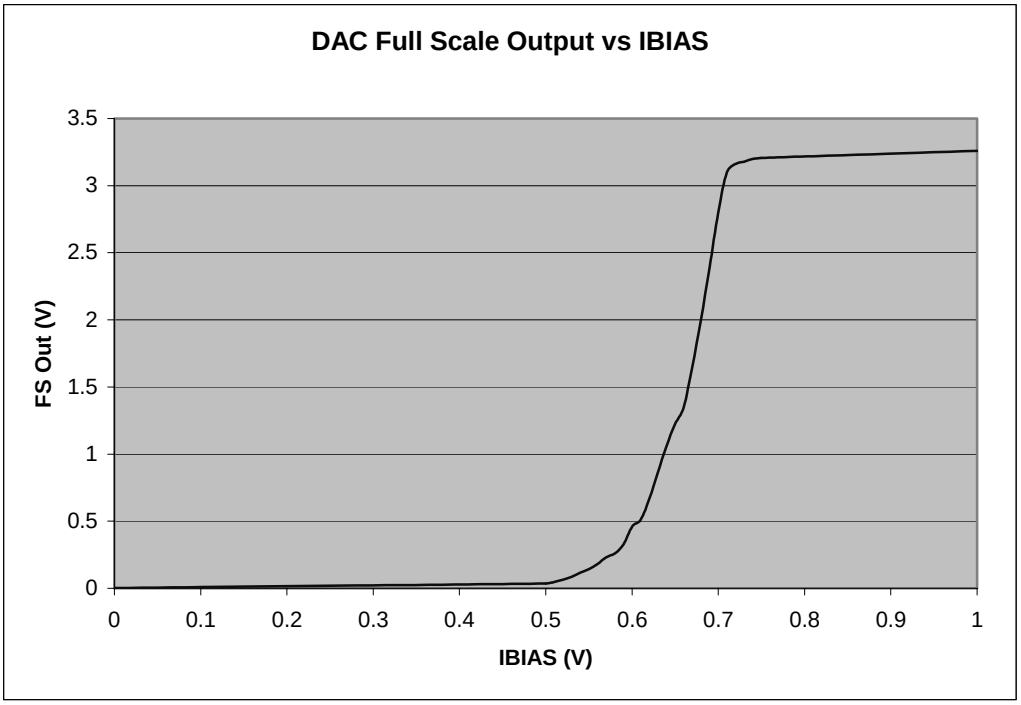


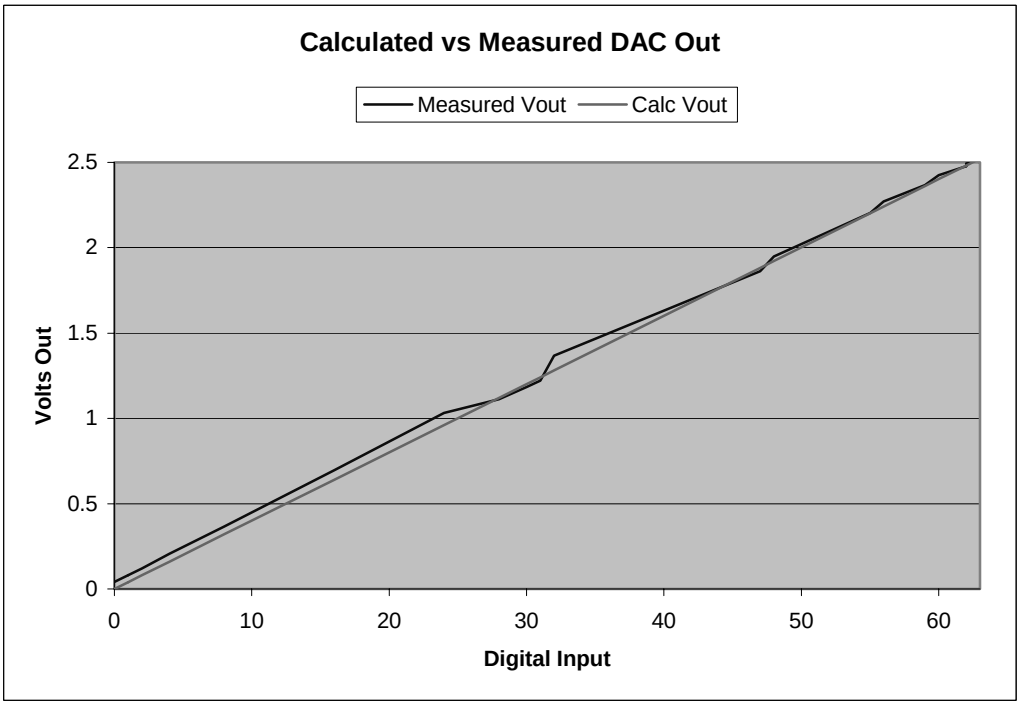
Fig. 6

At Goddard, we added a ring of substrate contacts around the perimeter and the six inverters shown at the top to allow single-ended command inputs.

Initial testing of the DAC showed a large sensitivity to the IBIAS voltage required to set the full scale range of the DAC. This voltage is applied directly to the gate of two NMOS transistors and so the threshold is greatly dependent upon process variations and temperature. Due to this fact, some circuitry will have to be added to this DAC in order for it to be useful in the ACD design. A plot of the DAC full-scale output versus the IBIAS voltage is shown below, showing the extremely sharp variation represented by this input voltage.



The following chart shows the measured voltage output of the DAC compared with the calculated voltage output for the same digital input. Variations in the Measured Vout may be due to bias voltage fluctuations in the power supply.



Tanner IO Pads

Tanner IO pads have ESD diodes intrinsic to the design. Using a Fluke multimeter in diode mode, the following diode drops were measured:

Pad to Vdd: 0.69 V
Pad to Gnd: 0.53 V

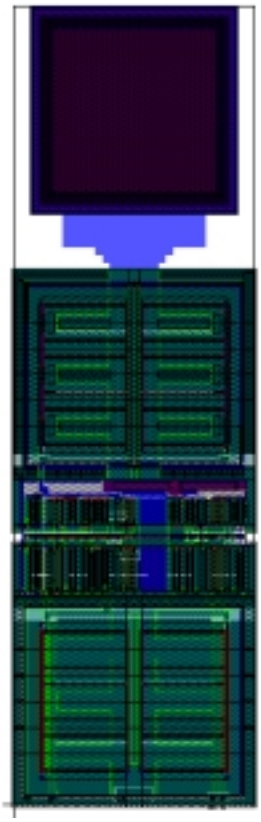


Fig. 7

ESD tolerance on these pads has not yet been measured. Drive strength and delay appear to be more than adequate for the ACD requirements.

Signal Propagation Delays and Rise Times:

Internal to the "mtest" logic, from the posedge of clock to the transition of the sync pulse, we measure approximately 5.25 ns logic propagation delay, as shown in the plot below in Fig. 8. The pulse rise time is measured at 2.3 nsec with a Tektronix TDS 744 500 MHz, 2 GS/sec digitizing oscilloscope with 500 MHz probes.

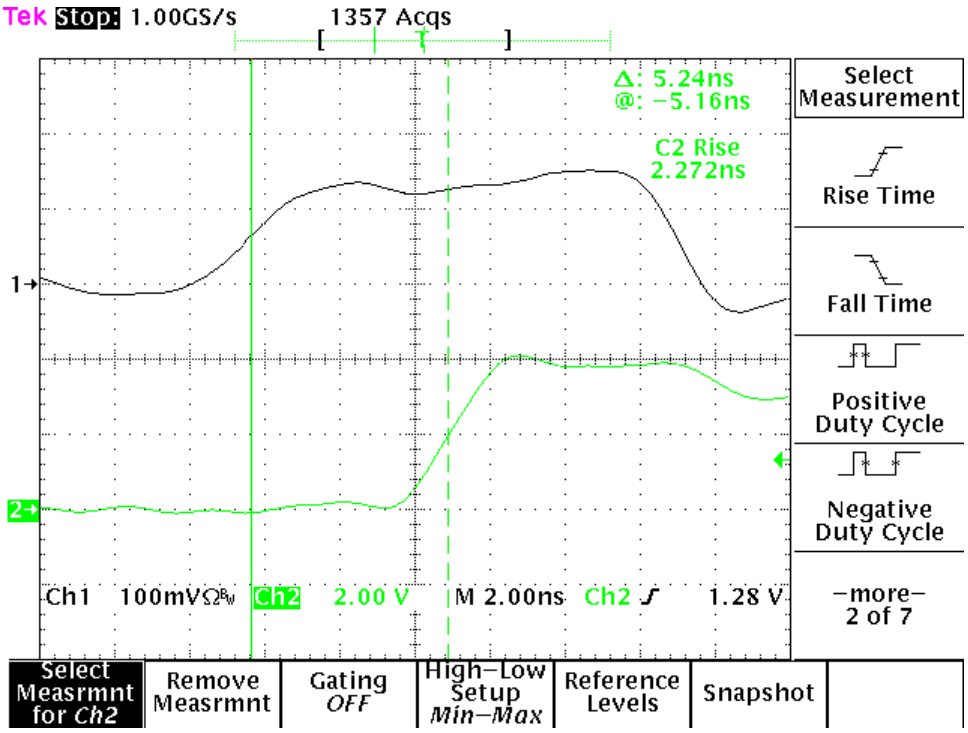


Fig. 8

An expanded view of these pulses is shcwn below in Fig. 9. It is clear from the plot that exact timing measurements are not possible due to probe lead inductance and bandwidth limitations. However, these measurements are sufficiently accurate for determination of general process suitability for use in the GLAST ACD ASICs.

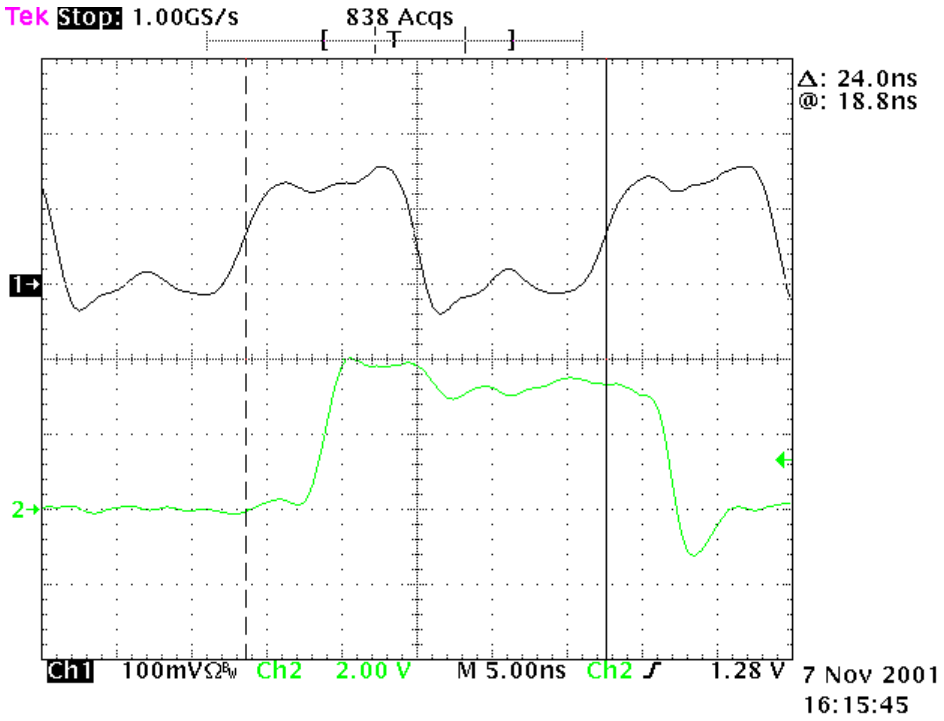
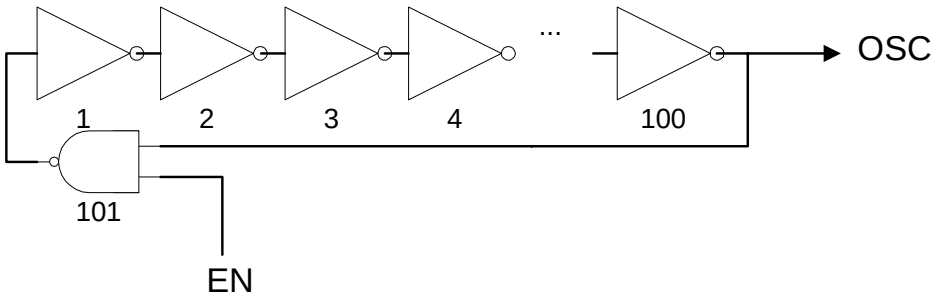


Fig. 9

Ring Oscillator Performance

The ring oscillator consists of the 100 inverters in series with a single NAND gate, as shown in the schematic below in Figures 10 and 11:



101 Stage Ring Oscillator with enable

Fig. 10

Fig. 11

This circuit was designed using the Tanner standard cell library (INV and NAND2) and found to operate correctly. At Vdd = 3.3V, this circuit oscillates at 41.5 MHz and at Vdd = 3.6V, the frequency is 45.4 MHz. At 3.3V, this translates to an internal propagation delay of 239 ps per gate. This oscillator is also available to run the "mtest" logic by feeding the clock back into the ASIC at pin K11. A plot of the clock and the P_SYNC_PLS_7 from pin K5 are shown below in Fig. 12.

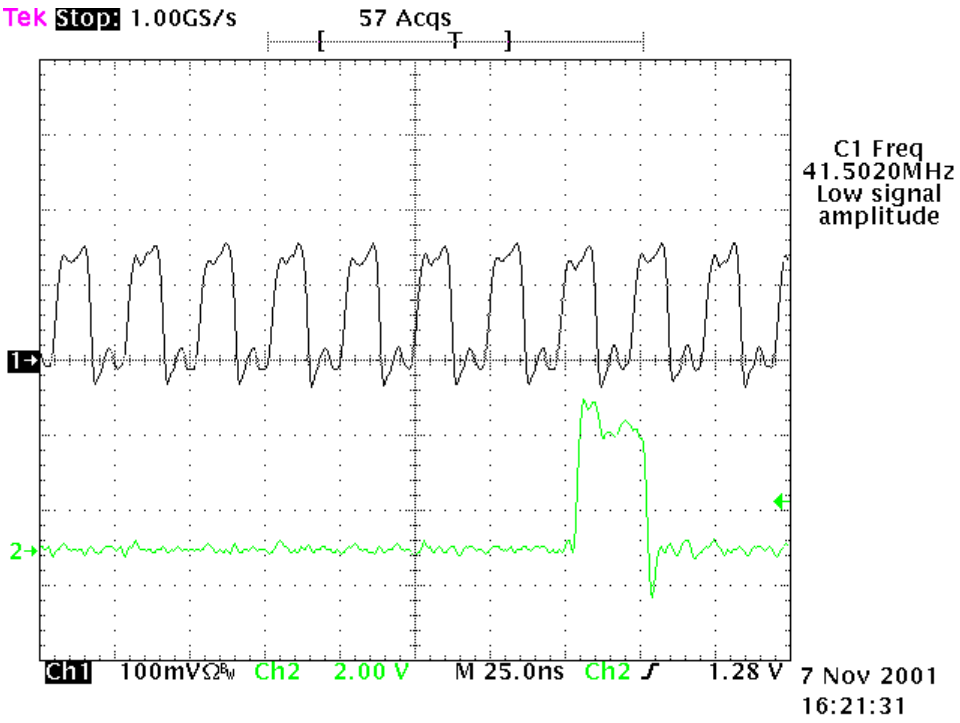


Fig. 12

The MOSIS 31-stage ring oscillator runs at 115.08 MHz, or giving a calculated gate delay of 280.3 ps per stage.

LVDS Driver and Reciever

Included on the ACDTEST2 chip are a LVDS driver and receiver combination. These modules were provided to Goddard by SLAC. These reside in the top right corner of the ASIC. The driver is shown in Fig. 13 below on the right, the receiver on the left.

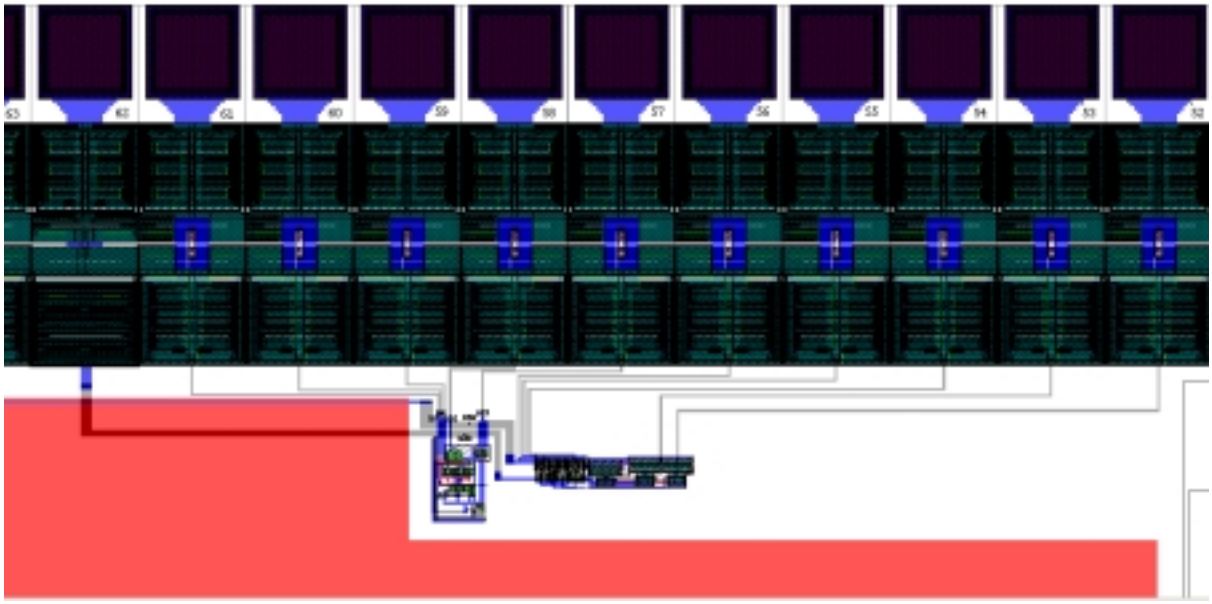


Fig. 13

The LVDS driver is shown below

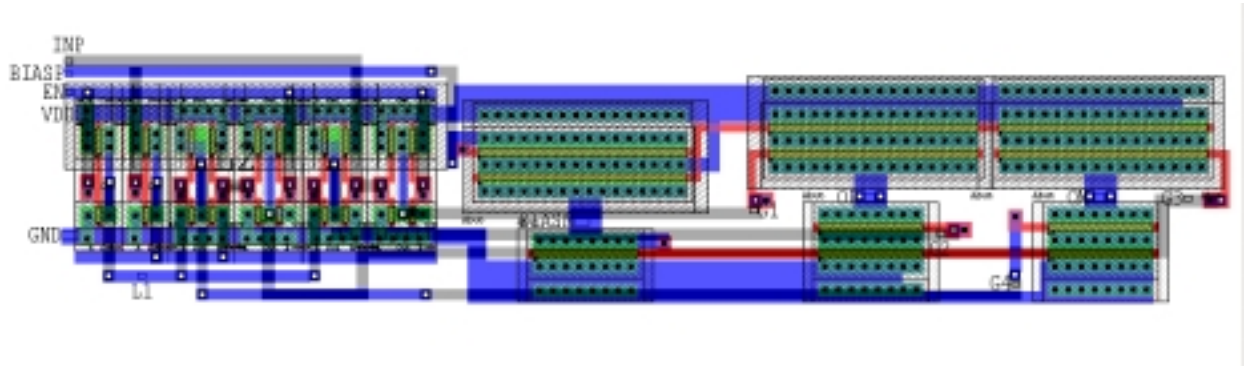


Fig. 14

The driver schematic is shown below in Fig. 15.

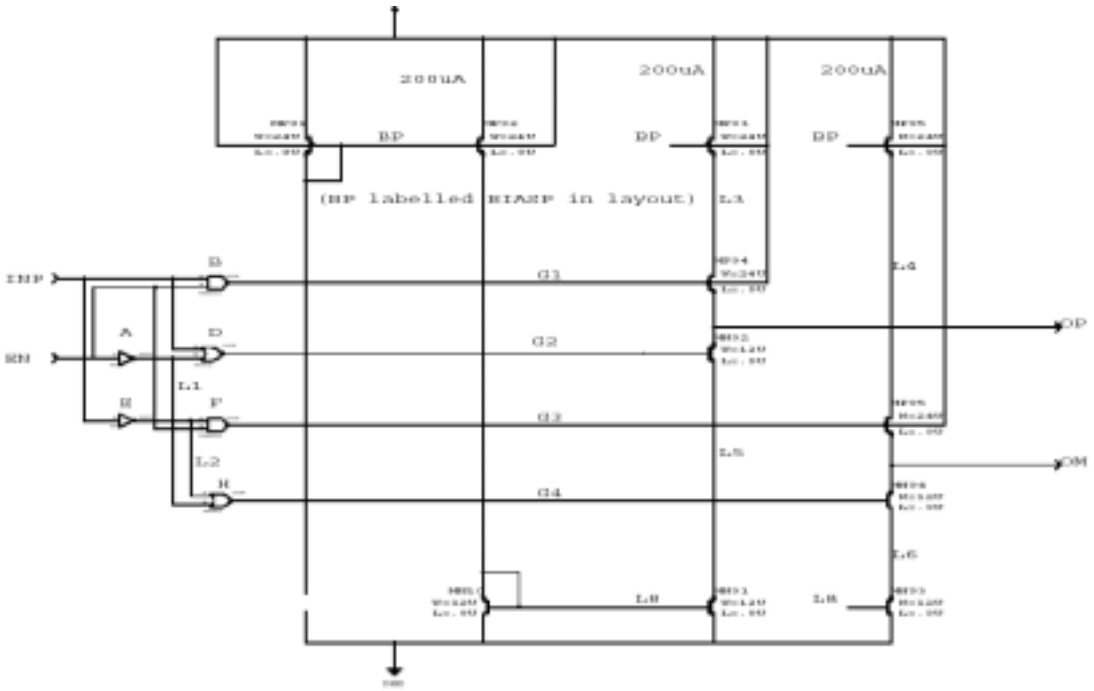


Fig. 15

The LVDS receiver is shown below in Fig. 16

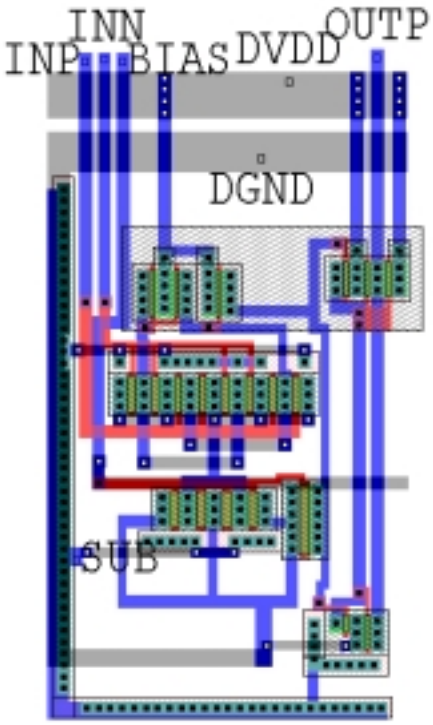


Fig. 16

The receiver schematic is shown below in Fig. 17.

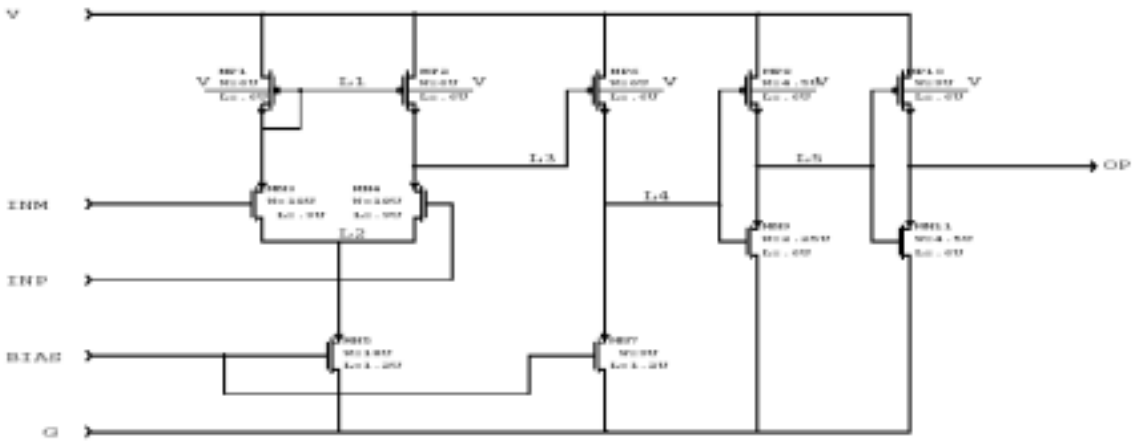


Fig. 17

The initial test of the LVDS driver and receiver pair was set up as shown below in Fig. 18

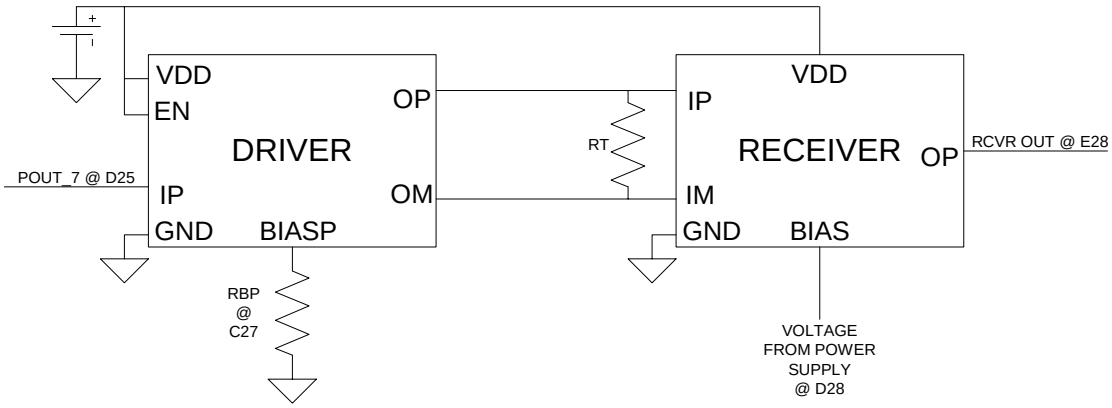


Fig. 18

The power, Vdd, was wired into the DAC Vdd power and the ground was connected to the ASIC ground. The driver input was connected to the POUT_7 output of the pseudo-random generator from MTEST. This provided a time-varying data stream for the input. This is shown on channel 2 (green) in Fig. 19.

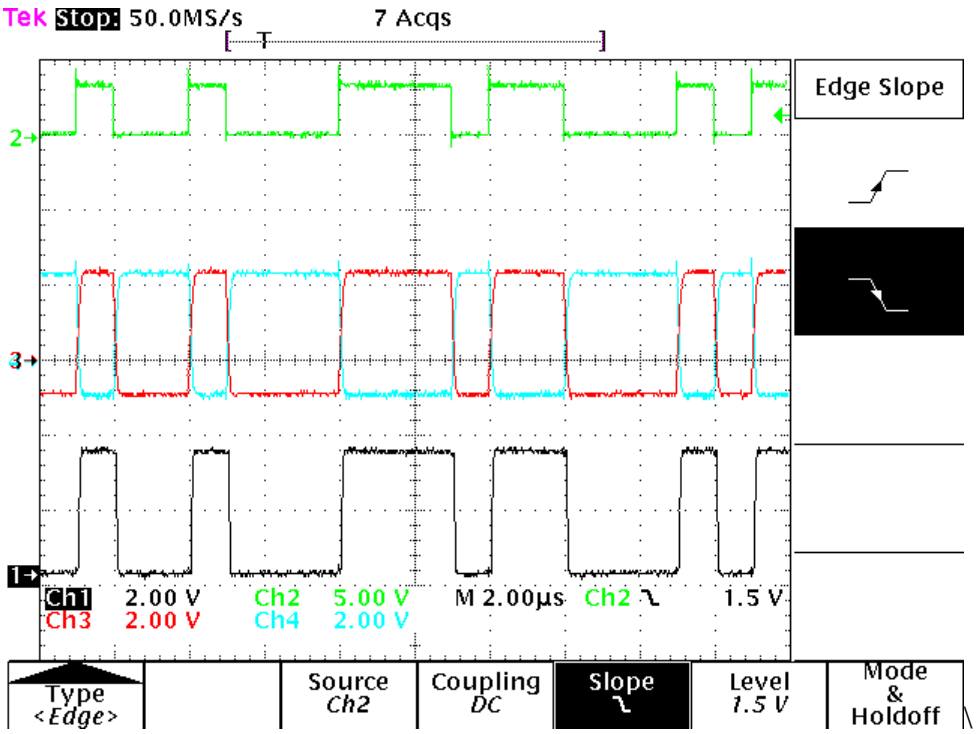


Fig. 19

The LVDS driver output is shown on channels 3 and 4. This plot was taken using a 1.14 mA driver bias current and a 330 Ω termination resistor, RT. The receiver bias voltage was 0.7V. The receiver output is shown on channel 1, the bottom trace.

This circuit was run using a slow clock (1 MHz) instead of the 41 MHz ring oscillator due to a design error on my part. The output of the LVDS receiver was connected through a standard, unbuffered Tanner IO pad (as were all the LVDS inputs and outputs). The loading combination of the pad impedance and the probe capacitance prohibited switching at the higher frequency clock. Even using a 0.6 pF probe showed the loading from the IO pad was significant. This rise time issue can be seen in the performance of channels 1, 3, and 4 below. Channel 2, the input, is from a buffered output pad and has a substantially better driver as evidenced by the improved rise time in Fig. 20 below. The scope is set to 100ns per division, indicating a rise time of about 50 ns with this load.

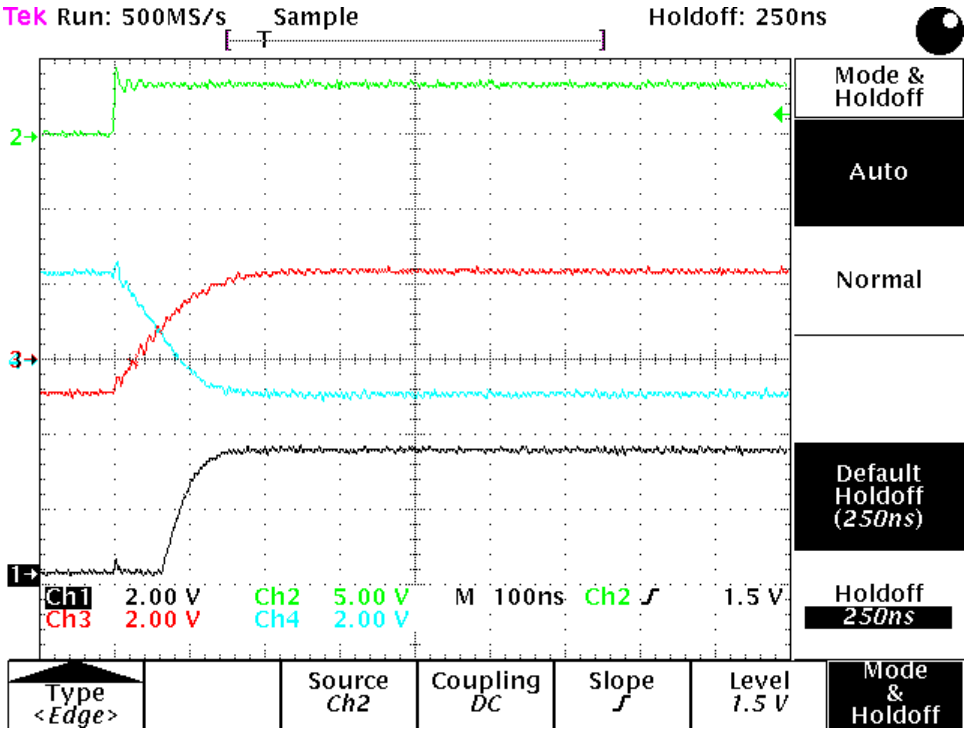


Fig. 20

Changing the driver bias current from 1.14 mA to 205 µA shows a further degradation in driver rise time, as expected. This is shown below in Fig. 21.

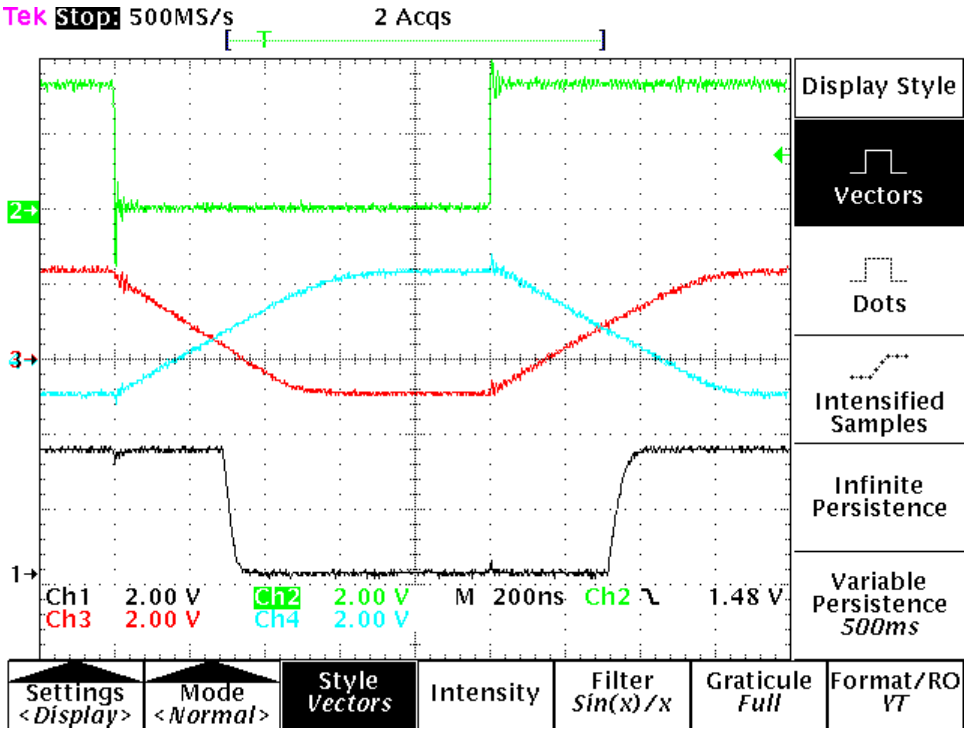


Fig. 21

Tests with the receiver bias voltage were as expected for an NMOS bias voltage. The minimum threshold voltage for operation was very nearly 0.60 V and operation continued up to 2.05V. As the receiver bias voltage was increased, the overall ASIC current draw increased until the NMOS transistor was saturated. In future designs, we will need to add a more stable means of biasing these drivers and receivers for them to be useful. It is anticipated that this will be a straightforward addition to these circuits.

Additionally, when the current range of the LVDS drivers was explored, it was found that the present circuit will not source more than about 1.45 mA, which is much less than the 3.5 mA required for the LVDS standard. We will either need a new driver cell from SLAC or we will have to create a new design which allows us to operate at the nominal current. Again, this should be a very straightforward modification.

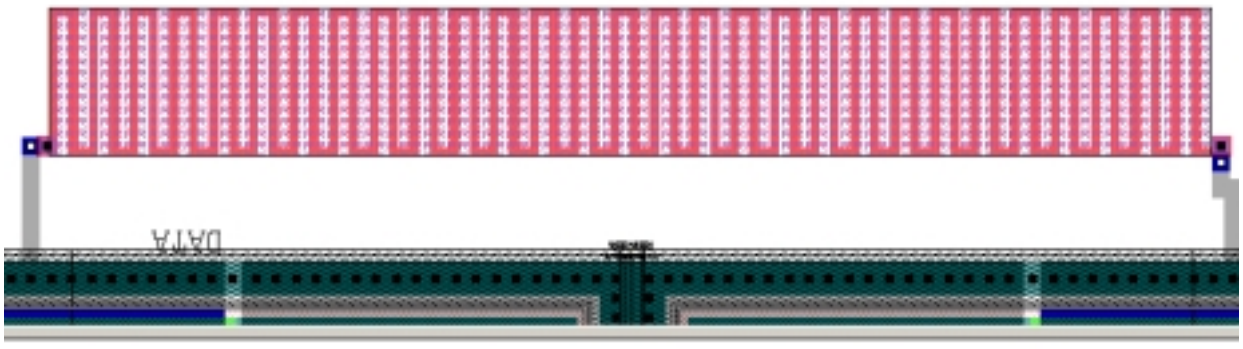
Variations of the polysilicon resistors

The resistance values of the poly resistors for each packaged part were measured and the results are tabulated below.

IC Number	Measured Resistance	Deviation from Average
1	3579.4 Ω	+10.07%
2	3149.6 Ω	-3.15%
3	3173.8 Ω	-2.40%
4	3068.6 Ω	-5.63%
5	3288.5 Ω	+1.12%

Average Resistance = 3251.98 Ω

The design of the poly resistor is shown below.



Each vertical leg is 37 λ and each horizontal segment between the vertical segments is 3 λ in length. There are 58 vertical segments and 58 horizontal segments, each 2 λ wide.

Using a resistance of 2.3 ohms per square from the process parameters, this calculates to be

$$2.3 * 58 * 39/2 = 2601.3\ \Omega,$$

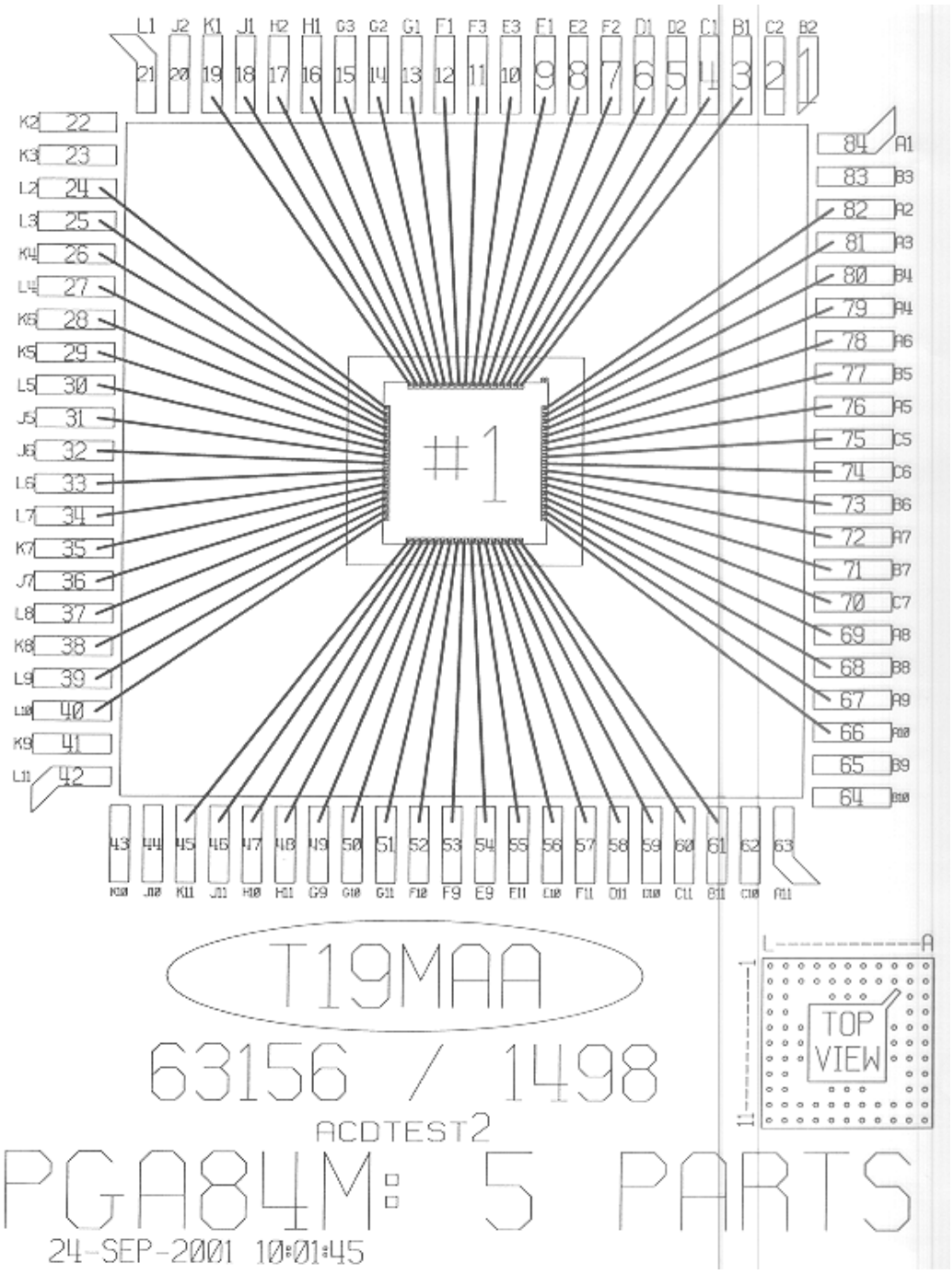
which is 20.0% lower than the average value observed. A calculation shows that the measured polysilicon resistance is nearer to 2.88 ohms-square.

Conclusions

The majority of our original for this ASIC were acheived. These include:

1. We have verified that our Exemplar synthesis toolset has the ability to successfully target the Agilent 0.5 μm library.
2. We have verified that the Tanner toolset can automatically place and route logic cells based on Exemplar EDIF input and that, to a first order, the Tanner standard cells are functional. The Tanner GDSII to MOSIS data transfer link is established.
3. We have established the ability to transfer a logic design initiated in Verilog-XL to working silicon.
4. We have verified that the Tanner IO pads function as expected. The pad drive circuitry and in-to-out delay are acceptable.
5. The ring oscillator functions as designed and provided a measure of propagation delay.
6. The SLAC digital-to-analog converter was verified to be functional. As with the LVDS circuitry, as more complete biasing network needs to be implemented. This should be added and tested in the next iteration of ASICs.
7. The LVDS driver and receiver circuits were functionally verified. Due to the design of the driver, it was not possible to verify functionality at the nominal 3.5 mA current. Due to the design of the output pad, it was not possible to verify functionality at the 20 MHz GARC clock frequency. Both of these items should be addressed in the next iteration of the digital logic.
8. Variations in poly-resistors were measured over five different ASICs. This was mainly done for my personal interest, but may be useful if we decide to implement on-chip poly resistors in a future design.

MOSIS Bonding Diagram for ACDTEST2



MOSIS PARAMETRIC TEST RESULTS

(from MOSIS web site based on probing of test structures on this wafer)

RUN: T19M VENDOR: AGILENT
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: SMSCN3MLC06_AG

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.9/0.6			
Vth		0.70	-0.87	volts
SHORT	20.0/0.6			
Idss		411	-174	uA/um
Vth		0.64	-0.87	volts
Vpt		10.0	-9.9	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.89	volts
Vjbkd		11.7	-9.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.68	0.46	V^0.5
K' (Uo*Cox/2)		77.0	-25.3	uA/V^2
Low-field Mobility		432.60	142.14	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask and etch bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL
SCN_SUBM (lambda=0.30), CMOSH, HP_CMOS14TB	-0.10
SCN (lambda=0.35)	-0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY+BLK	MTL1	MTL2	MTL3	UNITS
Sheet Resistance	2.7	2.3	2.2	113.3	0.07	0.07	0.05	ohms/sq
Contact Resistance	1.9	1.7	1.7			0.55	0.42	ohms
Gate Oxide Thickness	97							angstrom

PROCESS PARAMETERS	N_WELL	UNITS
Sheet Resistance	721	ohms/sq
Contact Resistance		ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	M1	M2	M3	N_WELL	UNITS
Area (substrate)	478	953	93	31	16	11	89	aF/um^2
Area (N+active)			3546					aF/um^2
Area (P+active)			3393					aF/um^2
Area (poly)				62	18	10		aF/um^2
Area (metal1)					43	15		aF/um^2
Area (metal2)						41		aF/um^2
Area (cap well)			2246					aF/um^2
Fringe (substrate)	315	173						aF/um
Overlap (N+active)			256					aF/um
Overlap (P+active)			250					aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	1.30	volts
Vinv	1.5	1.44	volts
Vol (100 uA)	2.0	0.18	volts
Voh (100 uA)	2.0	3.05	volts
Vinv	2.0	1.54	volts
Gain	2.0	-17.97	
Ring Oscillator Freq.			
DIV256 (31-stg,3.3V)		115.08	MHz
Ring Oscillator Power			
DIV256 (31-stg,3.3V)		0.20	uW/MHz/gate

COMMENTS: SUBMICRON

T19M SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Oct 26/01
* LOT: T19M WAF: 7130
  - Temperature_parameters=Default

.MODEL CMOSN NMOS (					
+VERSION	= 3.1	TNOM	= 27	LEVEL	= 49
+XJ	= 1.5E-7	NCH	= 1.7E17	TOX	= 9.7E-9
+K1	= 0.8075801	K2	= -0.0327314	VTH0	= 0.6496937
+K3B	= -6.198256E-3	W0	= 1E-5	K3	= 56.2528623
+DVT0W	= 0	DVT1W	= 0	NLX	= 3.800133E-8
+DVT0	= 6.7014491	DVT1	= 0.9174771	DVT2W	= 0
+U0	= 433.1075865	UA	= 1.702284E-12	DVT2	= -0.150909
+UC	= 1.644039E-11	VSAT	= 1.218978E5	UB	= 1.558712E-18
+AGS	= 0.1478242	B0	= 1.53122E-6	A0	= 0.900336
+KETA	= 3.328345E-3	A1	= 0	B1	= 5E-6
+RDSW	= 1.364581E3	PRWG	= 0.0163097	A2	= 1
+WR	= 1	WINT	= 2.129875E-7	PRWB	= -0.0740852
+XL	= -1E-7	XW	= 0	LINT	= 1.037651E-7
+DWB	= 7.579909E-9	VOFF	= -0.0691492	DWG	= -4.483271E-9
+CIT	= 0	CDSC	= 2.4E-4	NFACTOR	= 1.2720014
+CDSCB	= 0	ETA0	= 0.1134632	CDSCD	= 0
+DSUB	= 0.7146048	PCLM	= 0.6552182	ETAB	= 3.542439E-3
+PDIBLC2	= 5.154046E-4	PDIBLCB	= -0.5	PDIBLC1	= 2.10016E-3
+PSCBE1	= 6.719678E9	PSCBE2	= 7.656468E-10	DROUT	= 0.0282005
+DELTA	= 0.01	RSH	= 2.7	PVAG	= 0.1884228
+PRT	= 0	UTE	= -1.5	MOBMOD	= 1
+KT1L	= 0	KT2	= 0.022	KT1	= -0.11
				UA1	= 4.31E-9

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+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 2.56E-10       CGSO    = 2.56E-10       CGBO    = 1E-9
+CJ      = 5.081125E-4    PB      = 0.99           MJ      = 0.7886178
+CJSW    = 4.714954E-10   PBSW    = 0.99           MJSW    = 0.1
+CJSWG   = 2.2346E-10     PBSWG   = 0.99           MJSWG   = 0.1
+CF      = 0              PVTH0   = 7.788382E-3    PRDSW   = -49.2691828
+PK2     = 9.216985E-3    WKETA   = -4.805616E-3   LKETA   = -0.0113001
+PAGS    = 0.0968          )
*
.MODEL CMOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 9.7E-9
+XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = -0.8579444
+K1      = 0.3776787      K2      = 0.0244315      K3      = 71.436729
+K3B     = -4.6988777     W0      = 1E-5           NLX     = 2.508554E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 3.3421984      DVT1    = 0.4931879      DVT2    = -0.0325752
+U0      = 182.6938354    UA      = 1.331114E-9    UB      = 1.229664E-18
+UC      = -4.58451E-11   VSAT    = 1.871658E5     A0      = 1.0437638
+AGS     = 0.3061331      B0      = 4.301466E-6    B1      = 5E-6
+KETA    = 4.3991E-3      A1      = 0              A2      = 1
+RDSW    = 3.5E3          PRWG    = -0.0112683     PRWB    = 0.0195083
+WR      = 1              WINT    = 2.126142E-7    LINT    = 5.135708E-8
+XL      = -1E-7          XW      = 0              DWG     = -2.084096E-8
+DWB     = 5.566517E-9    VOFF    = -0.1042158     NFACTOR = 0.8202482
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.0528463      ETAB    = 3.606657E-3
+DSUB    = 0.2359412      PCLM    = 3.9701566      PDIBLC1 = 1.117975E-4
+PDIBLC2 = 5.25672E-3     PDIBLCB = 0.0660775      DROUT   = 8.45617E-7
+PSCBE1  = 8E10           PSCBE2  = 7.59459E-9     PVAG    = 10.7151924
+DELTA   = 0.01           RSH     = 2.3            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 2.5E-10        CGSO    = 2.5E-10        CGBO    = 1E-9
+CJ      = 9.452771E-4    PB      = 0.9473414      MJ      = 0.480677
+CJSW    = 1.774237E-10   PBSW    = 0.3948801      MJSW    = 0.11832
+CJSWG   = 4.256E-11      PBSWG   = 0.3948801      MJSWG   = 0.11832
+CF      = 0              PVTH0   = 3.688838E-4    PRDSW   = 270.0035945
+PK2     = 2.263316E-3    WKETA   = 9.143067E-3    LKETA   = -0.0121406
+PAGS    = 0.09532         )
*
```